

# ES\_LPC1764

Errata sheet LPC1764

Rev. 6 — 8 February 2011

Errata sheet

## Document information

Info	Content
<b>Keywords</b>	LPC1764 errata
<b>Abstract</b>	<p>This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.</p> <p>Each deviation is assigned a number and its history is tracked in a table at the end of the document.</p>



**Revision history**

Rev	Date	Description
6	20110208	<ul style="list-style-type: none"><li>Added Rev. A.</li></ul>
5	20110113	<ul style="list-style-type: none"><li>Added ADC.1 and PWM.1.</li></ul>
4	20100719	<ul style="list-style-type: none"><li>Added <math>V_{DD(REG)(3V3).1}</math>.</li></ul>
3	20100701	<ul style="list-style-type: none"><li>Added RTC.1.</li></ul>
2	20100316	<ul style="list-style-type: none"><li>The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Added I2S.1 and Ethernet.1.</li></ul>
1	20091014	<ul style="list-style-type: none"><li>Added MCPWM.1</li></ul>

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## 1. Product identification

The LPC1764 devices typically have the following top-side marking:

```
LPC1764xxx
xxxxxxx
xxYYWWR[x]
```

The last/second to last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC1764:

**Table 1. Device revision table**

Revision identifier (R)	Revision description
'.'	Initial device revision
'A'	Second device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

## 2. Errata overview

**Table 2. Functional problems table**

Functional problems	Short description	Revision identifier	Detailed description
RTC.1	The Real Time Clock (RTC) does not work reliably within the temperature specification.	'.'	<a href="#">Section 3.1</a>
I2S.1	XY divider will not work for PCLK-I2S higher than 74 MHz	'.', 'A'	<a href="#">Section 3.2</a>
Ethernet.1	Ethernet TxConsumeIndex register does not update correctly after the first frame is sent	'.', 'A'	<a href="#">Section 3.3</a>
PLL0.1	PLL0 (Main PLL) remains enabled and connected in Deep Sleep and Power-down modes	'.', 'A'	<a href="#">Section 3.4</a>
PCLKSELx.1	Peripheral Clock Selection Registers must be set before enabling and connecting PLL0	'.', 'A'	<a href="#">Section 3.5</a>
MCPWM.1	Input pins (MCI0-2) on the Motor Control PWM peripheral are not functional	'.'	<a href="#">Section 3.6</a>
V <sub>DD(REG)(3V3)</sub> .1	The minimum regulator supply voltage is 3.0 V for the temperature range -40 °C to 85 °C.	'.'	<a href="#">Section 3.7</a>
ADC.1	Internal sync inputs not operational.	'.', 'A'	<a href="#">Section 3.8</a>
PWM.1	When updating the duty cycle for PWM1.1 from 100 %, in some cases the output can stay low for a full PWM period before the update takes effect.	'.', 'A'	<a href="#">Section 3.9</a>

**Table 3. AC/DC deviations table**

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

### 3. Functional problems detail

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#### 3.1 RTC.1: The Real Time Clock (RTC) does not work reliably within the temperature specification

**Introduction:**

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. The RTC is clocked by a separate 32 kHz oscillator that produces a 1 Hz internal time reference. The RTC is powered by its own power supply pin, VBAT, which can be connected to a battery, externally tied to a 3 V supply, or left floating. The RTC can operate over temperature range from  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ .

**Problem:**

The RTC does not work reliably within the temperature specification.

**Work-around:**

None.

#### 3.2 I2S.1: The XY divider (8-bit Fractional Rate Divider) will not work for PCLK\_I2S (Peripheral clock for I2S) higher than 74 MHz

**Introduction:**

The transmitter/receiver MCLK (Master clock output) rate is generated using a fractional rate generator, dividing down the frequency of PCLK\_I2S. Values of the numerator (X) and the denominator (Y) must be chosen to produce a frequency twice that desired for the receiver MCLK, which must be an integer multiple of the receiver bit clock rate.

**Problem:**

The XY divider (8-bit Fractional Rate Divider) will not work for PCLK\_I2S (Peripheral clock for I2S) higher than 74 MHz.

**Work-around:**

Do not use PCLK\_I2S signal higher than 74 MHz.

### 3.3 Ethernet.1: Ethernet TxConsumeIndex register does not update correctly after the first frame is sent

#### Introduction:

The transmit consume index register defines the descriptor that is going to be transmitted next by the hardware transmit process. After a frame has been transmitted hardware increments the index, wrapping the value to 0 once the value of TxDescriptorNumber has been reached. If the TxConsumeIndex equals TxProduceIndex the descriptor array is empty and the transmit channel will stop transmitting until software produces new descriptors.

#### Problem:

The TxConsumeIndex register is not updated correctly (from 0 to 1) after the first frame is sent. After the next frame sent, the TxConsumeIndex register is updated by two (from 0 to 2). This only happens the very first time, so subsequent updates are correct (even those from 0 to 1, after wrapping the value to 0 once the value of TxDescriptorNumber has been reached)

#### Work-around:

Software can correct this situation in many ways; for example, sending a dummy frame after initialization.

### 3.4 PLL0.1: PLL0 (Main PLL) remains enabled and connected in Deep Sleep and Power-down modes

#### Introduction:

If the main PLL (PLL0) is enabled and connected before entering Deep Sleep or Power-down modes, main PLL (PLL0) automatically turns off and disconnects after the chip enters Deep Sleep mode or Power-down mode leading to reduced power consumption.

#### Problem:

If the main PLL (PLL0) is enabled and connected before entering Deep Sleep or Power-down modes, it will remain enabled and connected after the chip enters Deep Sleep mode or Power-down mode causing the power consumption to be higher.

#### Work-around:

In the software, user must disable and disconnect the main PLL (PLL0) before entering Deep Sleep and Power-down modes to reduce the power consumption. This must be done only if the main PLL (PLL0) was enabled and connected before entering Deep Sleep mode or Power-down mode.

The code below demonstrates the steps to disable and disconnect the main PLL0:

```
PLL0CON &= ~(1<<1);           /* Disconnect the main PLL (PLL0) */
PLL0FEED = 0xAA;              /* Feed */
PLL0FEED = 0x55;              /* Feed */
while ((PLL0STAT & (1<<25)) != 0x00); /* Wait for main PLL (PLL0) to disconnect */
PLL0CON &= ~(1<<0);           /* Turn off the main PLL (PLL0) */
PLL0FEED = 0xAA;              /* Feed */
PLL0FEED = 0x55;              /* Feed */
while ((PLL0STAT & (1<<24)) != 0x00); /* Wait for main PLL (PLL0) to shut down */
/***** Then enter into Deep sleep mode or Power-down mode*****/
```

### 3.5 PCLKSELx.1: Peripheral Clock Selection Registers must be set before enabling and connecting PLL0

**Introduction:**

A pair of bits in the Peripheral Clock Registers (PCLKSEL0 and PCLKSEL1) controls the rate of the clock signal that will be supplied to APB0 and APB1 peripherals.

**Problem:**

If the Peripheral Clock Registers (PCLKSEL0 and PCLKSEL1) are set or changed after PLL0 is enabled and connected, the value written into the Peripheral Clock Selection Registers may not take effect. It is not possible to change the Peripheral Clock Selection settings once PLL0 is enabled and connected.

**Work-around:**

Peripheral Clock Selection Registers must be set before enabling and connecting PLL0.

### 3.6 MCPWM.1: Input pins (MCI0-2) on the Motor Control PWM peripheral are not functional

**Introduction:**

On the LPC1764, the Motor Control PWM (MCPWM) peripheral is optimized for three-phase AC and DC motor control applications and can also be used in applications which require timing, counting, capture, and comparison. The MCPWM contains three input pins (MCI0-2) for PWM channels 0, 1, and 2. The inputs can be used as feedbacks for controlling brushless DC motors with Hall sensors, and also can be used to trigger a Timer/Counter's (TC) capture or increment a channel's TC when MCPWM is configured as a timer/counter.

**Problem:**

The input pins (MCI0-2) are not functional.

**Work-around:**

The GPIO interrupts on port 0 or port 2 can be used instead of the MCPWM MCI0-2 pins. The GPIO interrupts give the ability to trigger an interrupt on both the rising and falling edge; therefore, all six states of the connected hall sensor can be detected through an interrupt.

### 3.7 $V_{DD(REG)(3V3)}$ .1: The minimum regulator supply voltage is 3.0 V for the temperature range $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$

#### Introduction:

The device has a regulator supply voltage ( $V_{DD(REG)(3V3)}$ ) with a specification of 2.4 V to 3.6 V for the temperature range  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ .

#### Problem:

The device **does not work** when the regulator supply voltage ( $V_{DD(REG)(3V3)}$ ) is lower than 3.0 V for temperature range  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ .

#### Work-around:

Ensure that the  $V_{DD(REG)(3V3)}$  is kept above 3.0 V over the temperature range  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ .



### 3.8 ADC.1: External sync inputs not operational

**Introduction:**

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START	When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
	000	No start (this value should be used when clearing PDN to 0).	
	001	Start conversion now.	
	010	Start conversion when the edge selected by bit 27 occurs on the P2.10 / EINT0 / NMI pin.	
	011	Start conversion when the edge selected by bit 27 occurs on the P1.27 / CLKOUT / USB_OVRCRn / CAP0.1 pin.	
	100	Start conversion when the edge selected by bit 27 occurs on MAT0.1. Note that this does not require that the MAT0.1 function appear on a device pin.	
	101	Start conversion when the edge selected by bit 27 occurs on MAT0.3. Note that it is not possible to cause the MAT0.3 function to appear on a device pin.	
	110	Start conversion when the edge selected by bit 27 occurs on MAT1.0. Note that this does not require that the MAT1.0 function appear on a device pin.	
	111	Start conversion when the edge selected by bit 27 occurs on MAT1.1. Note that this does not require that the MAT1.1 function appear on a device pin.	

**Fig 1. A/D control register options**

**Problem:**

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on P2.10 or P1.27 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing a ADC trigger from GPIO) is estimated as follows:

- For PCLK\_ADC = 120 MHz, probability error = 12 %
- For PCLK\_ADC = 50 MHz, probability error = 6 %
- For PCLK\_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

**Work-around:**

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

### 3.9 PWM.1: When updating the duty cycle for PWM1.1 from 100 %, in some cases the output can stay low for a full PWM period before the update takes effect

#### Introduction:

On the LPC17xx PWM peripheral, two match registers can be used to provide a single edge controlled PWM output. One match register (PWM1MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. As an example, match register PWM1MR1 controls PWM1's edge position. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when a PWM1MR0 match occurs.

#### Problem:

Only in single-edge mode, if the duty cycle for PWM1.1 (Pulse Width Modulator 1, channel 1 output) is updated from 100 % (PWM1MR1 = PWM1MR0), then the output for PWM1.1 could unexpectedly remain low for a full PWM period before the new desired duty cycle takes effect. This problem only affects the output for PWM1.1. Other PWM channels (PWM1.2 to PWM1.6) are not affected by this problem.

#### Work-around:

A software fix can be implemented where the user can load PWM1MR1 with  $\text{PWM1MR0} + 1$  (at least 1) to avoid any delays in the PWM1.1's output update.

## 4. AC/DC deviations detail

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### 4.1 n/a

## 5. Legal information

### 5.1 Definitions

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